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Title: CLOCK DISTRIBUTION MODULE (155Y503007) USER'S MANUAL

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Clock Distribution Module Overview

The SNS Clock Distribution Module (CDM) Rev. AM is based on the Los Alamos National Laboratory (LANL) Low-Energy Demonstration Accelerator (LEDA) CDM design, with the frequencies adjusted appropriately. The CDM provides synchronized clocks to the various RFCS control modules, all derived from (and phase-locked to) the 10-MHz reference provided from the master oscillator. Before producing the 40-MHz analog-to-digital converter (ADC) clock, the 10-MHz signal is first phase-aligned with the 50-MHz intermediate frequency (IF) reference at each system. The CDM design supports either one or two RF control systems in the same VXIbus crate without modification.

Physically, the CDM is a single-wide VXIbus-compliant module using both the P1 and P2 backplane connectors. RF connectors are PKZ blind-mate connectors, in D-subminiature housings, from the Phoenix Company of Chicago. Test points are included on the front panel to monitor the various clock signals and to provide a 10-MHz output that can be used as a source for synchronizing an RF generator, if need be. Weight and power consumption of the module are **TBD**.

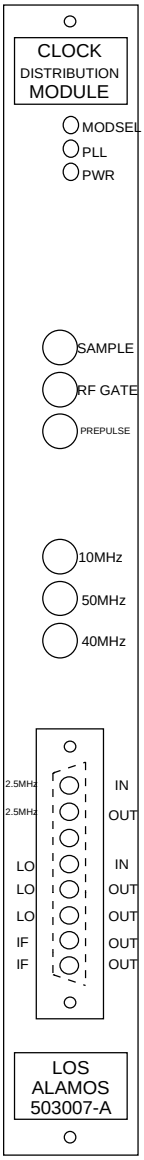
The input signals required by the CDM are a 10-MHz clock and a 50-MHz IF reference. The CDM realigns the leading edge of the 10-MHz synchronous time marker (SYNCH) with the 50-MHz IF reference, and then generates a 40-MHz ADC clock. Both the 10-MHz and 40-MHz clocks are emitter-coupled logic (ECL) clocks, which drive the ECL clock lines on the back plane. The test points for the 10-MHz SYNCH, the 40-MHz clock, and the 50-MHz IF signal are available on the front panel. These are LEMO connectors and require 50-ohm terminated test cables.

To use the CDM in a test lab setup, synchronize the 10-MHz clock (square-wave, 500 mV p-p) and the IF reference signal (0 dBm) to J7 contacts #1 and #4, turn on the crate power, and observe the frequency outputs from the LEMO test ports and the distribution port J7. At this time, the LED indicators for both the power and the phase-locked loop (PLL) clock should be green.

CDM Architecture

CDM Revision AM uses a PLL oscillator to generate a 40-MHz ADC clock synchronous with the 10-MHz time marker. The 10-MHz input comes from the master oscillator and is phase-locked to the 50-MHz IF reference signal from the reference line in the tunnel via a D-flip-flop. This insures that any phase error with the 10-MHz frequency from the distribution is corrected. The bandwidth of the PLLs is currently relaxed to its maximum — about 15 kHz. When needed, the bandwidth can easily be narrowed down by increasing the value of a few capacitors in the loop. For a more detailed description of the RF Reference-Distribution System, see LANL Technical Note LANSCE-5-TN-00-017 (LA-UR-00-4374), "Phase Stability Requirements for the SNS Reference Distribution System."

CDM Signal Inputs/Outputs



Front Panel Inputs	Signal Level	Connector–Frequency
IF_REF_IN	Into 50 Ω (J7 contact #4) +0 dBm nominal +3 dBm maximum) -3 dBm minimum	PKZ—50 MHz
10MHz_IN	Into 50 Ω (J7 contact #1) 0 dBm nominal (about 500 mV p-p) 200 mV p-p minimum 1 V p-p maximum (because of ECL limit)	PKZ—10 MHz
PREPULSE*	TTL from Timing Module	LEMO 50 Ω—N/A
RF_GATE*	TTL from Timing Module	LEMO 50 Ω—N/A
SAMPLE*	TTL from Timing Module	LEMO 50 Ω—N/A

Note: A square wave is preferable for better edges.

Note: The 10-MHz clock must be inherently synchronous with the 50-MHz IF frequency because both the 10-MHz and the IF frequency are derived from a common 2.5-MHz clock source in the master oscillator. Therefore, for a test setup, the two frequency generators for the 10-MHz and the 50-MHz signals must be synchronized through the reference frequency input/output of the instruments.

Front Panel Outputs	Signal Level	Frequency
IF_OUT (x2)	+10 dBm into 50 Ω	PKZ—50-MHz reference
10MHz_OUT	+10 dBm into 50 Ω	PKZ—10-MHz reference
10_MHz	**TBD** dBm into 50 Ω	LEMO 50 Ω—10-MHz reference test point
40_MHz	**TBD** dBm into 50 Ω	LEMO 50 Ω—40-MHz ADC Clock test point
50_MHz	**TBD** dBm into 50 Ω	LEMO 50 Ω—50-MHz IF test point

Note: The 50-MHz IF output of the current revision (Rev. AM) is not a perfect sine wave because the signal source outputs a kind of square wave and there is no filter in the signal path to kill the harmonics. We suggest that you use one or two in-line 50-MHz low-pass filters from Mini-Circuits (LP-50) at the output to suppress the unwanted harmonics. With one LP-50 filter, the second and third harmonic levels in the output should be lower than -60˚dB. The future revision will have this filter built in**.**

Backplane Outputs	Functionality When Driven	Backplane
40 MHz	ADC Sampling Clock	ECLTRG0
SYNCH (10 MHz)	I/Q Synchronization Pulse	ECLTRG1
SAMPLE*	Sample I/Q Data	TTLTRG0*
RF_GATE*	Carrier enable for LLRF	TTLTRG3*
PREPULSE*	RF pulse timing fiducial	TTLTRG4*
FAULT_L*	RF Shutdown Fault (Left)	TTLTRG5*
FAULT_R*	RF Shutdown Fault (Right)	TTLTRG7*

Table 1 shows the connectors for the RF signals.

Table 1. CDM PKZ Connector-Pin Assignments

Pin	Function	Pin	Function
1	REF_IN (10 MHz)	5	Not used
2	REF_OUT (10 MHz)	6	Not used
3	NOT USED	7	IF_OUT_1 (50 MHz)
4	IF_REF_IN (50 MHz)	8	IF_OUT_2 (50 MHz)

Front Panel Indicators (LEDs) normal/fault colors:

MODSEL: Yellow — Lit when the CDM is selected by the input/output controller (IOC). Stretched to 10 ms for visibility.

PLL_LOCK: Green/red — Red when the PLL oscillator becomes unlocked.

PWR_SUPPLY: Green/Red — Green when the VXIbus crate external voltages are within tolerance.

CDM VXIbus INTERFACE

Configuration Registers:	**Value**	**Bits**
DEVICE CLASS	Extended	01_2
ADDRESS SPACE	A16	00_2
MANUFACTURER ID	4000	$FA0_{16}$
REQUIRED MEMORY	N/A	N/A
MODEL CODE	3915	$F4B_{16}$

VXIbus Compatibility:	
DEVICE CLASS	Extended Register-Based
DEVICE TYPE	Servant-only
LOGICAL ADDRESS SELECTION	Static Switch Configuration (Set to D0)
INTERRUPTER	Programmable

EPICS Interface

Table 2 defines the CDM VXIbus A16 address space, while Table 3 defines the CDM status and control register.

Table 2. CDM A16 Address Space

BYTE OFFSET	REGISTER NAME	VALUE
00_{16}	LANL MANUFACTURER'S ID	$7FA0_{16}$
02_{16}	DEVICE TYPE	$FF4B_{16}$
04_{16}	STATUS/CONTROL	$XXXX_{16}$ see below
06_{16}	OFFSET	0000_{16}
08_{16}	ATTRIBUTE	$XXX7_{16}$
$0A_{16}$	SERIAL NUMBER HIGH	0000_{16}
$0C_{16}$	SERIAL NUMBER LOW	$00XX_{16}$
$0E_{16}$	VERSION NUMBER	$000A_{16}$
10_{16}		$FFFF_{16}$
12_{16}		$FFFF_{16}$
14_{16}		$FFFF_{16}$
16_{16}		$FFFF_{16}$
18_{18}		$FFFF_{16}$
$1A_{16}$		$FFFF_{16}$
$1C_{16}$		$FFFF_{16}$
$1E_{16}$		$FFFF_{16}$
20_{16}		$FFFF_{16}$
22_{16}		$FFFF_{16}$
24_{16}		$FFFF_{16}$
26_{16}		$FFFF_{16}$
28_{16}		$FFFF_{16}$
$2A_{16}$		$FFFF_{16}$
$2C_{16}$		$FFFF_{16}$
$2E_{16}$		$FFFF_{16}$
30_{16}		$FFFF_{16}$
32_{16}		$FFFF_{16}$
34_{16}		$FFFF_{16}$
38_{16}		$FFFF_{16}$
$3A_{16}$		$FFFF_{16}$
$3C_{16}$		$FFFF_{16}$
$3E_{16}$		$FFFF_{16}$

The CDM uses four of the status bits to tell EPICS when any of the three PLLs has failed, or when a power supply has failed. Low = Fail, high = OK. See Table 3.

Table 3. CDM Status Word

Bit 15	Bit 14	Bit 13	Bit 12	Bits 11–8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bits 1–0
0	MODID*	Reserved	Prdy	Not used	PWR FAIL	10 PLL FAIL	50 PLL FAIL	40 PLL FAIL	Ready	Passed	Reserved

CDM Built-in Test

Front-panel LEDs indicate the health of the module. Loop-lock indicators verify that the PLLs are indeed locked and putting out power. The backplane voltages provided by the VXIbus backplane are monitored. The "all OK" indicator is a green LED; the light will turn red should one or more of these lines fail. All of this information (excluding Loop Power Out) is also placed in the status/control register for communicating these

conditions to the operator via EPICS. The CDM is, in many ways, a very simple module. It monitors the health of its loops at all times and flags the operator if one or more should fail.

CDM Calibration

Each module will be calibrated before use to compensate for module-to-module variations in amplitude and phase to insure that all modules are interchangeable to the control system.

Timing between 2.5 MHz and LO for Avoiding Metastability

TBD

CDM Power Requirements TBD

+24 VDC
+12 VDC
+5 VDC
-2 VDC
-5.2 VDC
-12 VDC
-24 VDC

CDM Build Matrix

TBD